

Appl. No. 10/603,570
Amdt. Dated November 22, 2006
Reply to Office Action of September 15, 2006

Attorney Docket No. 81707.0186
Customer No. 26021

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REMARKS/ARGUMENTS:

Claims 1 and 9 are amended. Support for the amendments to claims 1 and 9 can be found at p. 16, lines 10-13 of the Applicant's specification. Claims 1 and 4-12 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

The present invention relates to a thermoelectric module having excellent thermoelectric characteristics that can be used for cooling heat-generating members such as semiconductors and optical integrated circuits, and to a process for producing the same. (Applicant's specification, at p. 1, lines 6-10).

PRIORITY:

Applicant acknowledges Office's statement that a certified copy of the 2002-186853 application has not been filed as is required by 35 U.S.C. § 119(b). Applicant respectfully submits that a certified copy of the 2002-186853 application will be submitted to the Office at a date no later than the payment of the issue fee.

CLAIM REJECTIONS UNDER 35 U.S.C. § 103:

Claims 1, 7, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cauchy et al. (U.S. Patent No. 6,103,967) in view of Fuschetti (U.S. Patent No. 5,429,680). The Applicant respectfully traverses the rejection as to amended claim 1. Claim 1, as amended, is as follows.

A thermoelectric module comprising support substrates, a plurality of wiring conductors formed on the opposing surfaces of the support substrates, a plurality of thermoelectric elements, and solder layers formed between said wiring conductors and said thermoelectric elements, wherein the total projected area (Sv) of voids contained in said solder layers projected onto the surfaces of the support substrates

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on the side where the solder layers are in contact via the wiring conductors is from 1 to 20% of the total area (St) of the surfaces on where the solder layers are in contact with the wiring conductors, wherein said thermoelectric elements are provided with plated layers on the surfaces in contact with the solder layers, wherein said plated layers are formed by plating with nickel and gold, wherein the plated layer formed by plating with gold has a thickness of 0.01 to 10 μm .

Applicant respectfully submits that the cited references cannot render amended claim 1 obvious, because the cited references fail to teach or suggest that "the plated layer formed by plating with gold has a thickness of 0.01 to 10 μm ."

It is an aspect of the present invention that upon forming Au-plated layers 7b on the nickel-plated layers 7a, enhanced wettability is exhibited to the solder paste and, as a result, junction strength to the solder layers 6 and reliability are easily improved. It is desired that the Au-plated layers 7b have a thickness of 0.01 to 10 μm by taking into consideration the cost of the material and a drop in the workability due to the ductility of Au in addition to wettability. (Applicant's specification, at p. 16, lines 6-13).

The Office acknowledges that Cauchy "only discloses nickel-plated layers" and relies on Fuschetti for teaching a thermoelectric device with a gold layer. However, the gold layer of Fuschetti has a thickness of about 0.001 to about 0.008 inch. (Fuschetti, column 5, lines 19-26). About 0.001 to about 0.008 inch is equivalent to 25 to 200 μm . This range is outside of the 0.01 to 10 μm range of amended claim 1. Consequently, the benefits discussed above are not achieved.

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claim 1 obvious, because the cited references fail to teach or suggest each and every claim limitation. Claims 7 and 8 depend from

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claim 1 and cannot be rendered obvious for at least the same reasons as claim 1. Withdrawal of this rejection is thus respectfully requested.

Claims 4-6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cauchy in view of Fuschetti as applied to claims 1, 7, and 8 above, and further in view of Zhu (Thermal Impact of Solder Voids in the Electronic Packaging of Power Devices, 15th IEEE SEMI-THERM Symposium, 1999, pgs 22-29) and Lau et al. (Effects of Voids on Bump Chip Carrier (BCC++) Solder Joint Reliability, 2002 Electronic Components and Technology Conference, May 28-31 2002, pgs 992-1000). The Applicant respectfully traverses this rejection.

Claims 4-6 depend from claim 1 and therefore, cannot be rendered obvious over Cauchy and Fuschetti for at least the same reasons discussed above. Zhu cannot remedy the defect of Cauchy and Fuschetti and is not relied upon by the Office for such. Instead, the Office cites Zhu for teaching an average thickness for the solder layer of 50 μm ; and for teaching void percentages less than 20% maintain extremely low variations in thermal transmission through the solder and distributed shallow voids, produce the lowest amount of thermal variations. Lau, similarly, cannot remedy the defect of Cauchy and Fuschetti and is not relied upon by the Office for such. Instead, the Office cites Lau for teaching void sizes of 25, 50, and 75 μm and showing the effect these sizes have on crack formation within the solder layer. Neither Zhu nor Lau teach or suggest the use of a gold metallized layer of any kind much less one having a thickness of 0.01 to 10 μm .

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claims 4-6 obvious, because the cited references fail to teach or suggest each and every claim limitation. Withdrawal of this rejection is thus respectfully requested.

Claims 9-12 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Cauchy in view of Fuschetti, Lau and Jafri (U.S. Patent No. 4,895,606). The

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Applicant respectfully traverses this rejection as to amended claim 9. Claim 9, as amended, is as follows:

A process for producing a thermoelectric module having at least support substrates, a plurality of wiring conductors formed on the opposing surfaces of the support substrates and a plurality of thermoelectric elements, by applying a solder paste containing a void-forming agent onto the surfaces of either the wiring conductors or the thermoelectric elements in the thermoelectric module, and joining said wiring conductors and said thermoelectric elements together by a heat treatment, wherein said thermoelectric elements are provided with plated layers on the surfaces in contact with the solder paste, wherein said plated layers are formed by plating with nickel and gold, wherein the plated layer formed by plating with gold has a thickness of 0.01 to 10 μm .

Claim 9, as amended, requires that the plated layer formed by plating with gold has a thickness of 0.01 to 10 μm . Consequently, claim 9 is patentable over Cauchy, Fuschetti, and Lau for the reasons discussed above. Jafri cannot remedy the defect of Cauchy, Fuschetti, and Lau and is not relied upon by the Office for such. Instead, the Office cites Jafri for teaching formulations for soldering flux. Jafri fails to teach or suggest the use of a gold metallized layer of any kind much less one having a thickness of 0.01 to 10 μm .

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claim 9 obvious, because the cited references fail to teach or suggest each and every claim limitation. Claims 10-12 depend from claim 9 and cannot be rendered obvious for at least the same reasons as claim 9. Withdrawal of these rejections is thus respectfully requested.

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Applicant believes the foregoing amendments comply with requirements of form and thus may be admitted under 37 C.F.R. § 1.116(b). Alternatively, if these amendments are deemed to touch the merits, admission is requested under 37 C.F.R. § 1.116(c). In this connection, these amendments were not earlier presented because they are in response to the matters pointed out for the first time in the Final Office Action.

Lastly, admission is requested under 37 C.F.R. § 1.116(b) as presenting rejected claims in better form for consideration on appeal.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4600 to discuss the steps necessary for placing the application in condition for allowance.

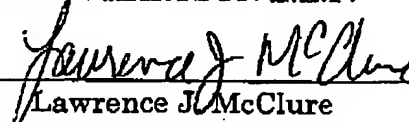
If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: November 22, 2006

By:


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